

MS7004

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CPU:

Intel Northwood/Prescott
Up to 3.6GHz

System Chipset:

PM800/PT800 (North Bridge)
VIA 8237 (South Bridge)

On Board Chipset:

BIOS -- ISA EEPROM
AC'97 Codec --ALC655
LPC Super I/O -- W83697HF
LAN -- PHY RTL8201
CLOCK -- CY28341-3

Main Memory:

DDR * 2 (Max 2GB)

Expansion Slots:

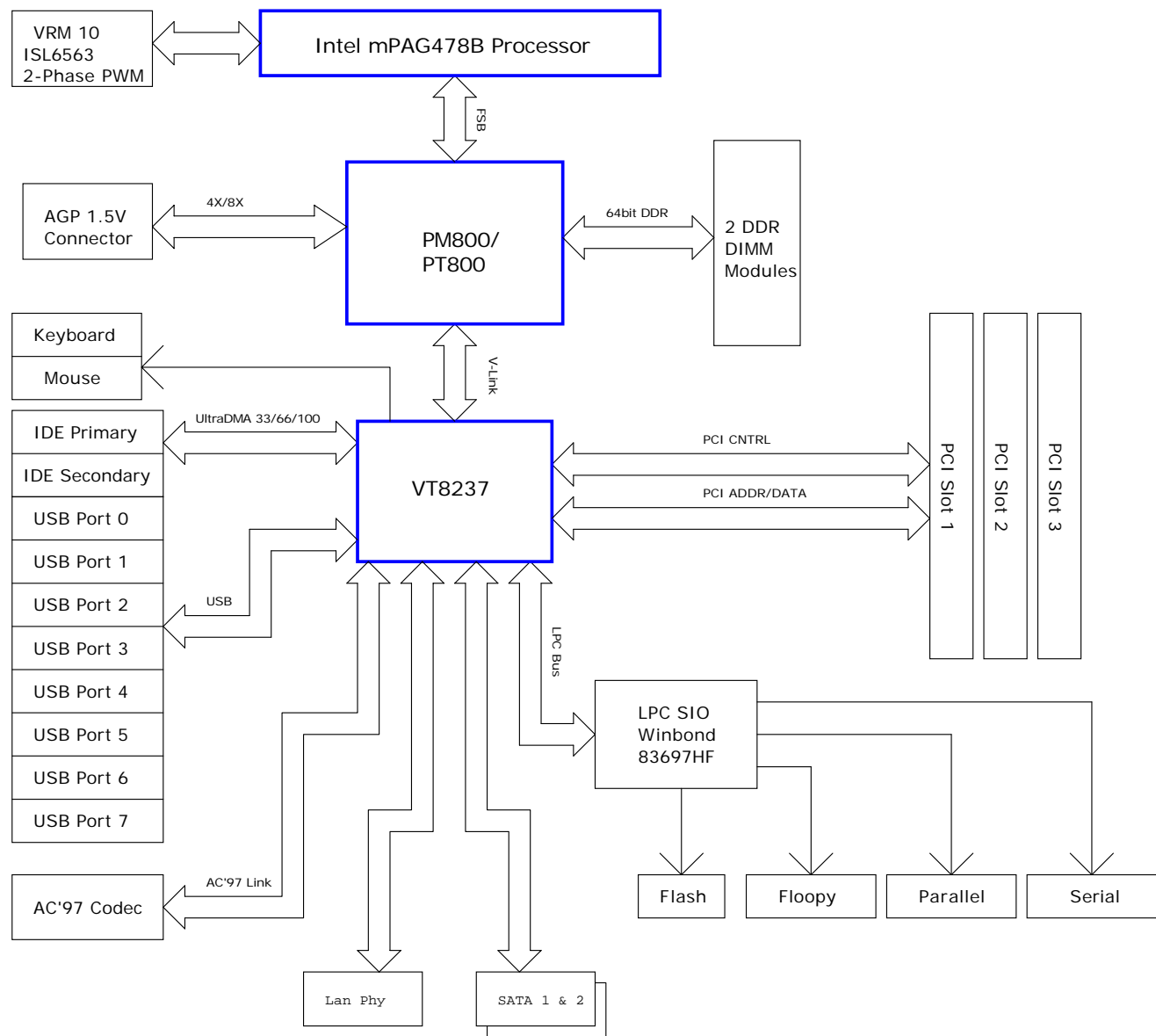
AGP * 1
PCI2.3 SLOT * 3
CNR * 1

PWM:

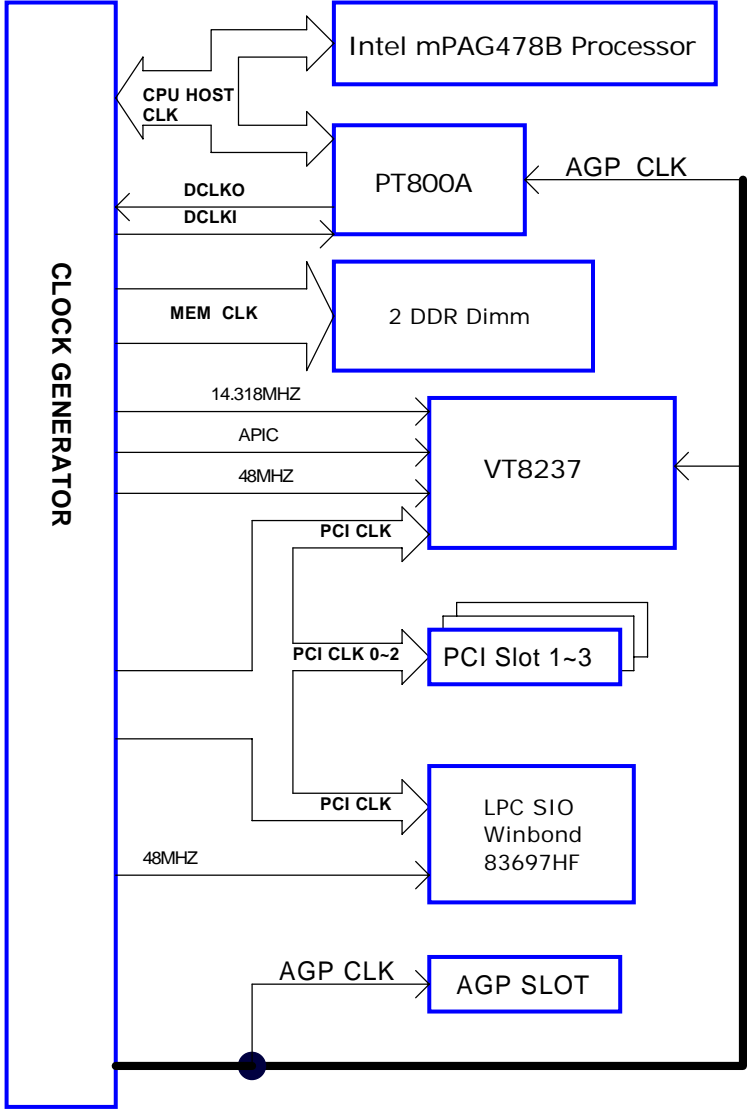
Controller: STL6710

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Title COVER SHEET				
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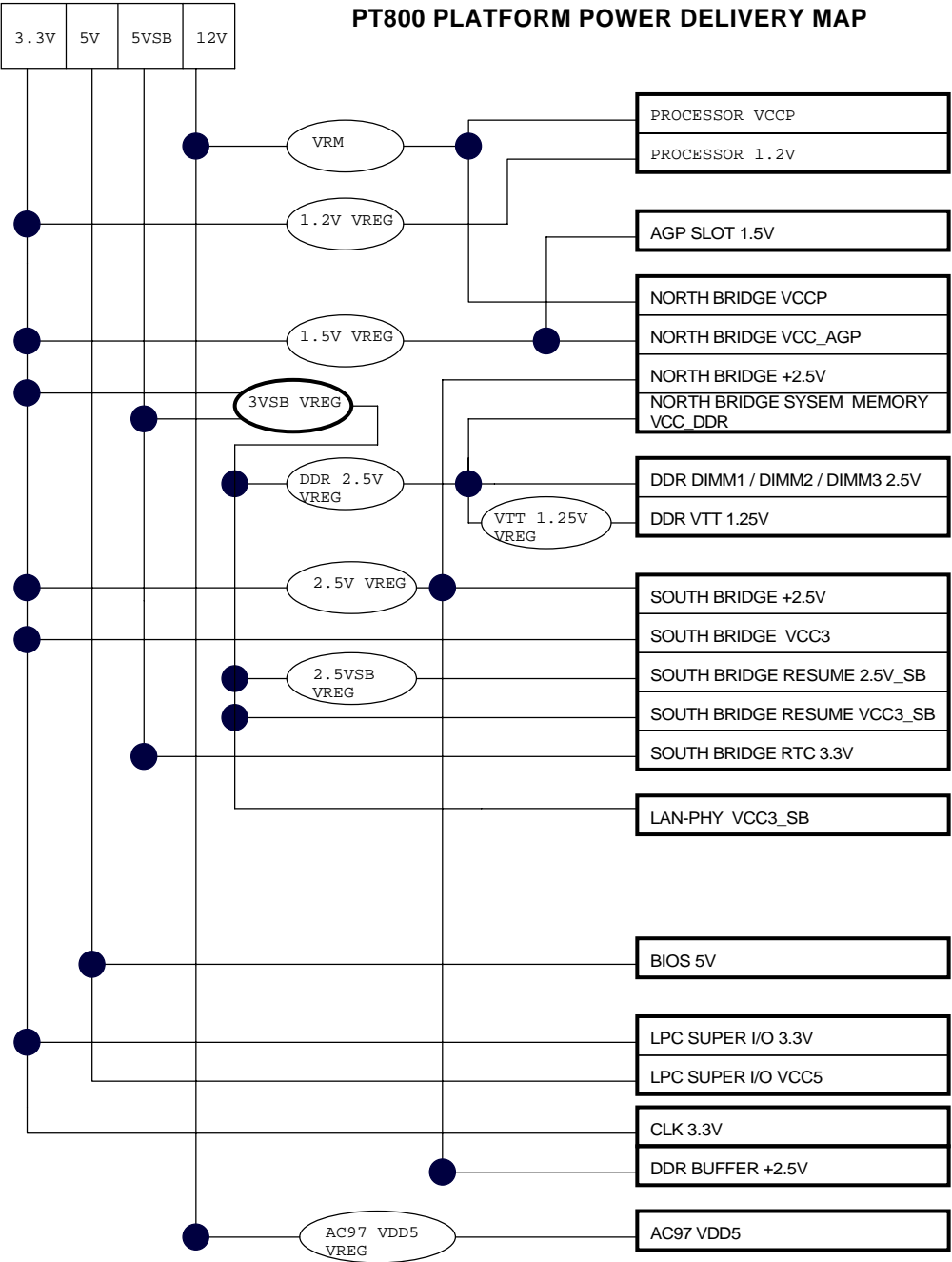
Block Diagram



PT800 PLATFORM CLOCK GENERATOR MAP



PT800 PLATFORM POWER DELIVERY MAP



NB

GPIO Pin	Type	Function	Power well
GPI 0	I	GPI 0	RESUME
GPI 1	I	IDE2 CBD	RESUME
GPO 0	I	GPO 0	RESUME
GPO 1	I	GPO 0	RESUME
GPIO A	I	NB STR S	MAIN
GPIO B	I	IOQ DEPH	MAIN
GPIO C	I	NB STR S	MAIN
GPIO D	I	GTL PULL	MAIN

I/O

GPIO 10	I/O	HI	MAIN
GPIO 11	I/O	HI	MAIN
GPIO 12	I/O	HI	MAIN
GPIO 13	I/O	NA	MAIN
GPIO 14	I/O	NA	MAIN
GPIO 15	I/O	NA	MAIN
GPIO 16	I/O	NA	MAIN
GPIO 17	I/O	NA	MAIN
GPIO 18	I/O	NA	MAIN
GPIO 19	I/O	NA	MAIN
GPIO 20	I/O	NA	MAIN
GPIO 21	I/O	NA	MAIN
GPIO 22	I/O	NA	MAIN

default output
default output
default output

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Slot 1	INTA# INTB# INTC# INTD#	PCI_REQ#0 PCI_GNT#0	AD19	PCICLK0	18 (PCI_CLK0)
PCI Slot 2	INTB# INTC# INTD# INTA#	PCI_REQ#1 PCI_GNT#1	AD20	PCICLK1	19 (PCI_CLK1)
PCI Slot 3	INTC# INTD# INTA# INTB#	PCI_REQ#2 PCI_GNT#2	AD21	PCICLK2	21 (PCI_CLK2)
PCI Slot 4	INTD# INTA# INTB# INTC#	PCI_REQ#3 PCI_GNT#3	AD22	PCICLK3	14 (PCI_CLK3)
PCI Slot 5	INTA# INTB# INTC# INTD#	PCI_REQ#4 PCI_GNT#4	AD23	PCICLK4	17 (PCI_CLK4)

FWH

GPIO Pin	Type	Function
GPI 0	I	Pull UP through 1K ohms (unused)
GPI 1	I	Pull UP through 1K ohms (unused)
GPI 2	I	Pull UP through 1K ohms (unused)
GPI 3	I	Pull UP through 1K ohms (unused)
GPI 4	I	Pull UP through 1K ohms (unused)

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	MCLK0/MCLK#0 MCLK1/MCLK#1 MCLK2/MCLK#2
DIMM 2	1010001B	MCLK3/MCLK#3 MCLK4/MCLK#4 MCLK5/MCLK#5
DIMM 3	1010010B	MCLK6/MCLK#6 MCLK7/MCLK#7 MCLK8/MCLK#8

PCI RESET DEVICE

Signals	Target
PCIRST#1	SB, NB
PCIRST#2	PCI slot 1-3, 1394, FWH
HD_RST#	Primary, Scondary IDE

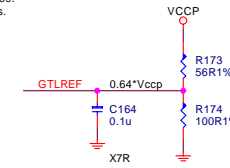
CPU SIGNAL BLOCK

VIDPWRGD DC Specifications

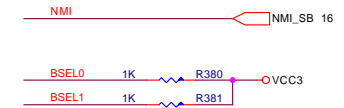
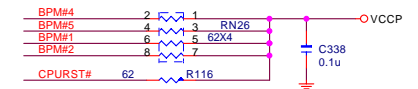
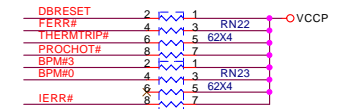
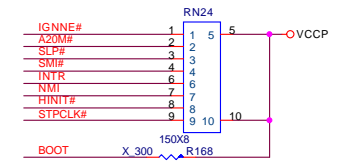
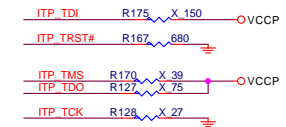
	Min	Typ	Max
VIL			0.3
VIH	0.9		

It must route to the enable pin of PWM and CK-409.
VIDGD to Vccp delay time is from 1ms to 10ms.
VIDGD rising time is 150ns.

CPU GTL REFERENCE VOLTAGE BLOCK

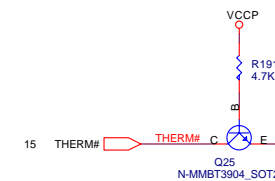
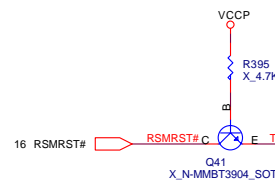


CPU ITP BLOCK



CPU STRAPPING RESISTORS

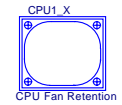
ALL COMPONENTS CLOSE TO CPU

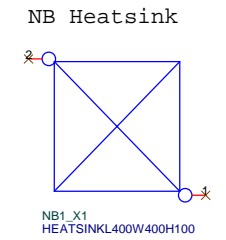
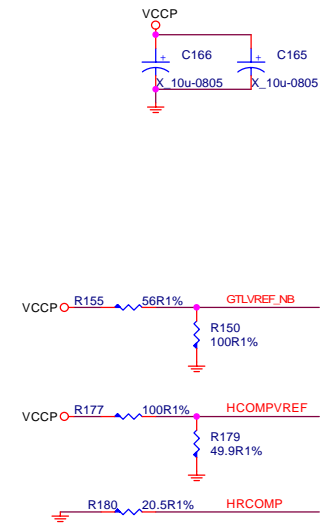
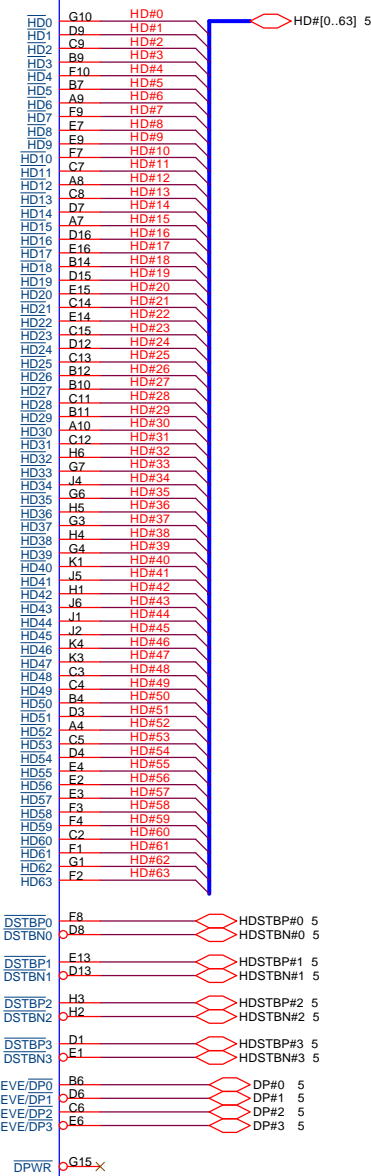
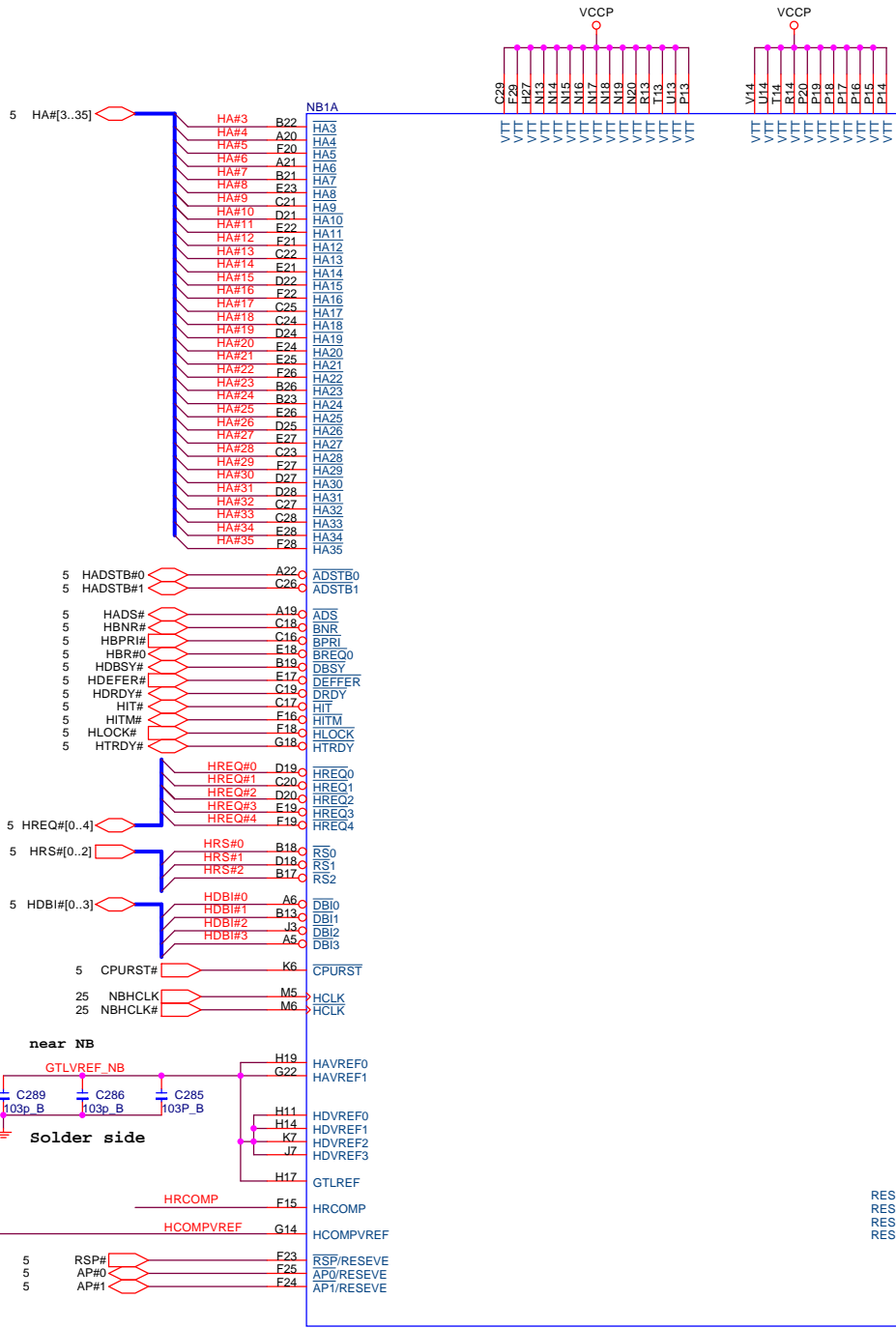


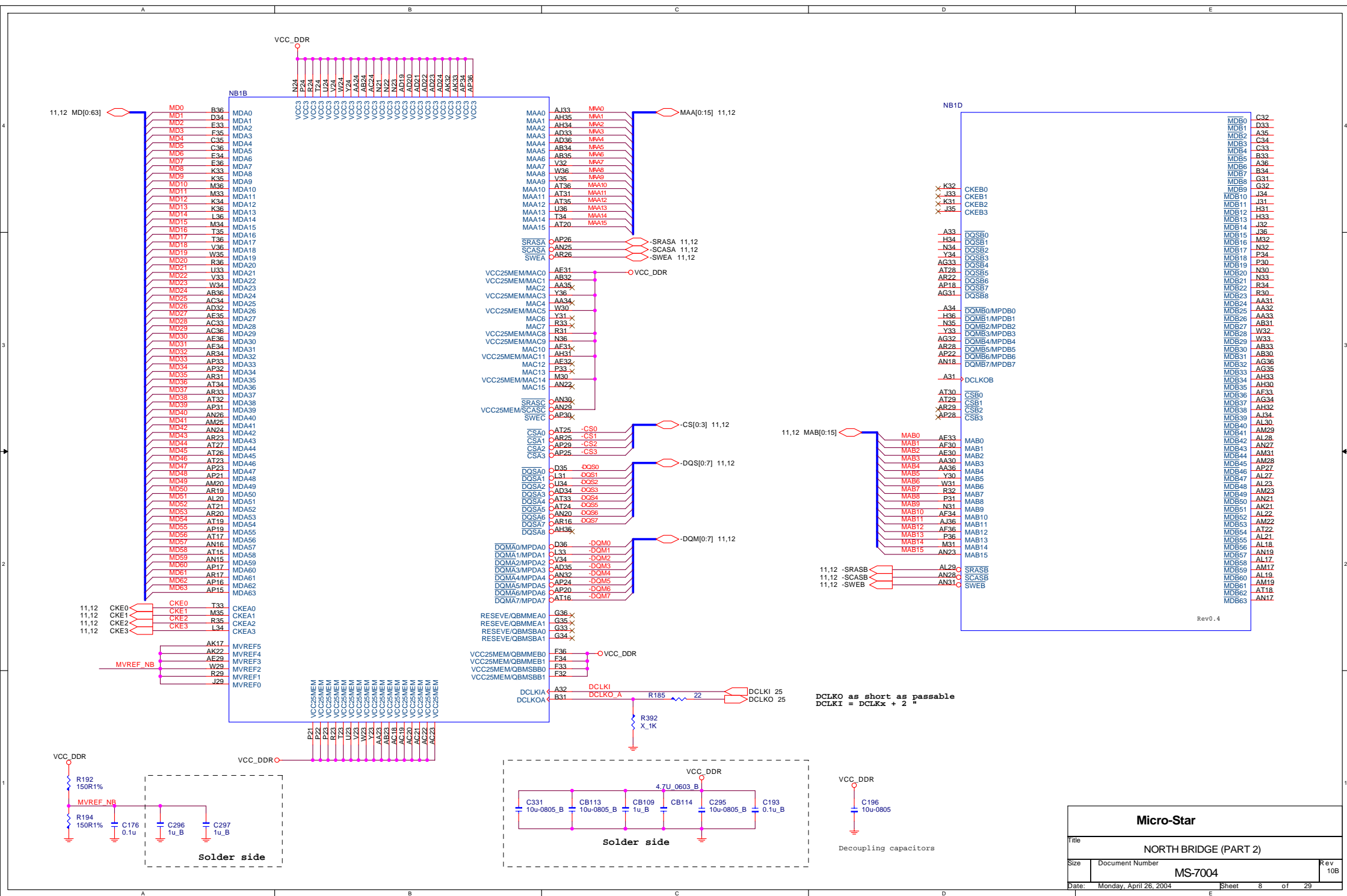
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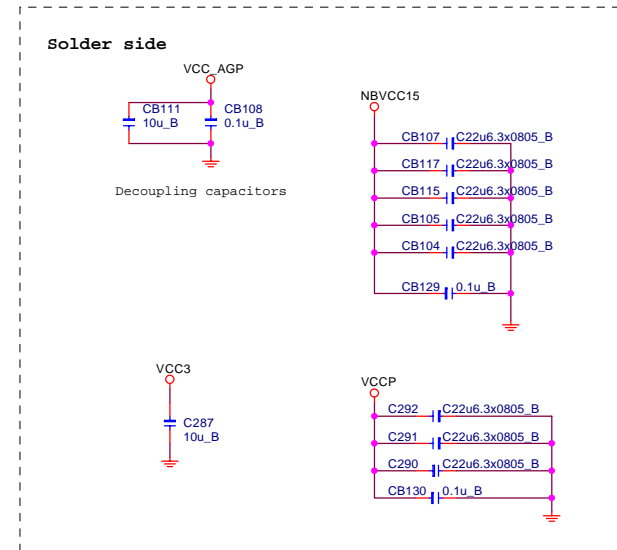
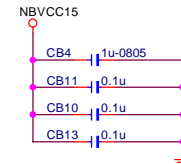
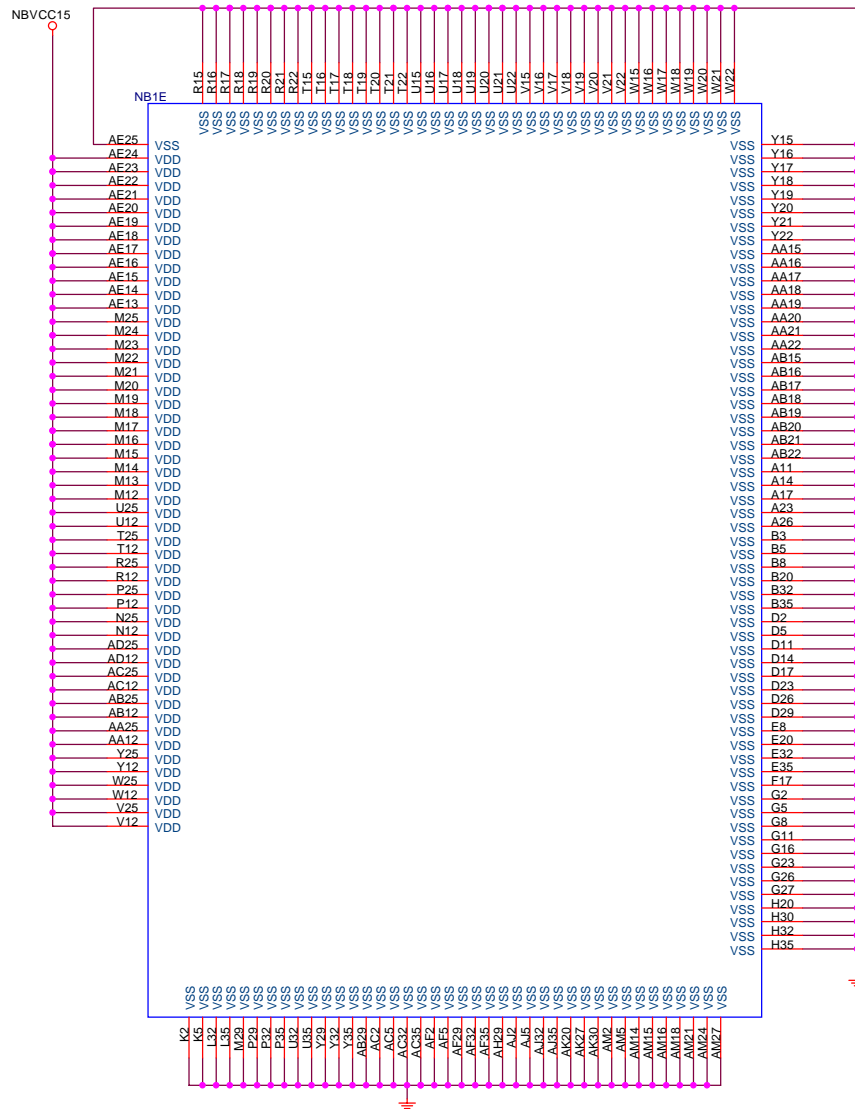
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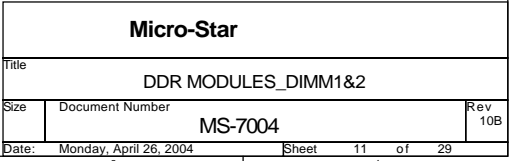
The figure contains two circuit diagrams. The left diagram, labeled '1000', shows a VCCP input connected to a series of capacitors: C179, C178, C177, C158, C147, and C22u-1206. The right diagram, labeled '10000', shows a VCCP input connected to a series of capacitors: C282, C281, C337, C113, C114, C115, C116, C117, C118, and C10u-1206. Both diagrams show a VCCP input connected to a series of capacitors leading to ground.

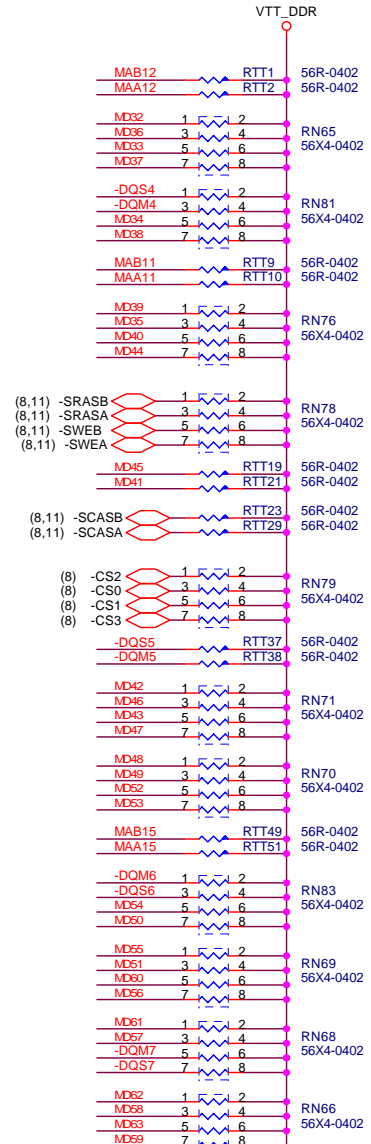
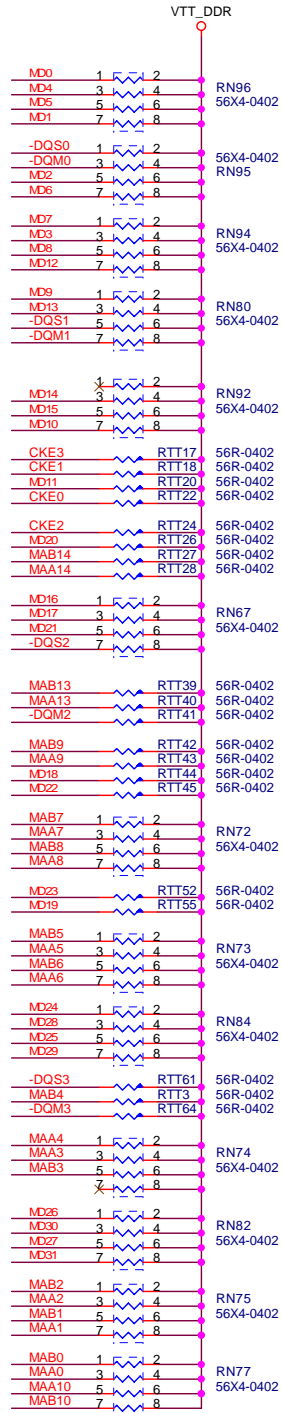
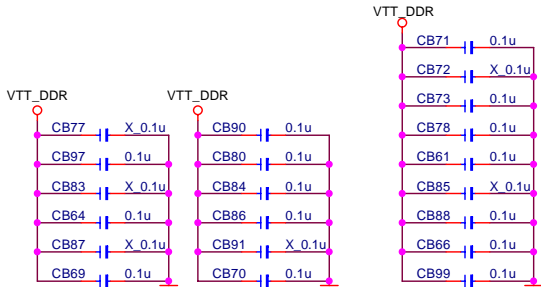
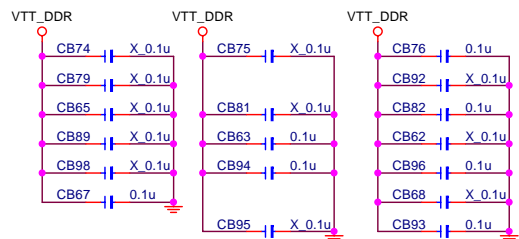
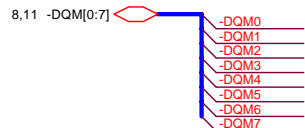
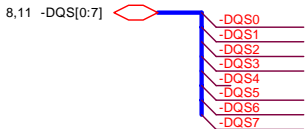
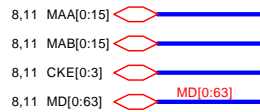




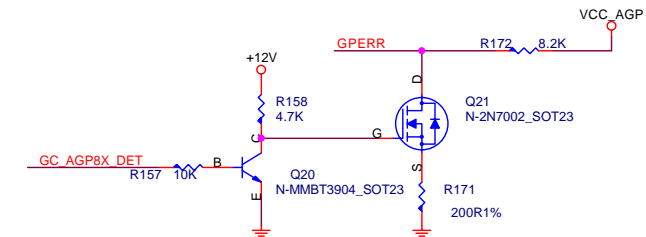
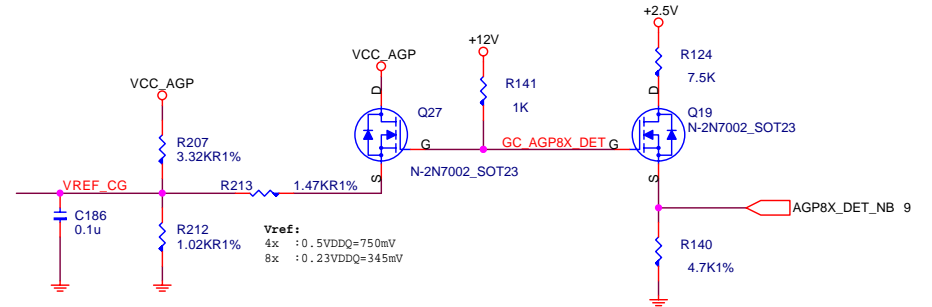
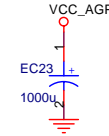
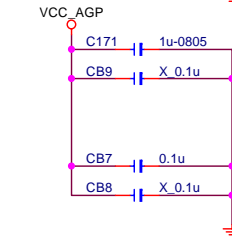
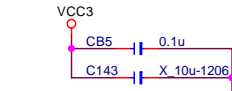
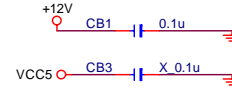
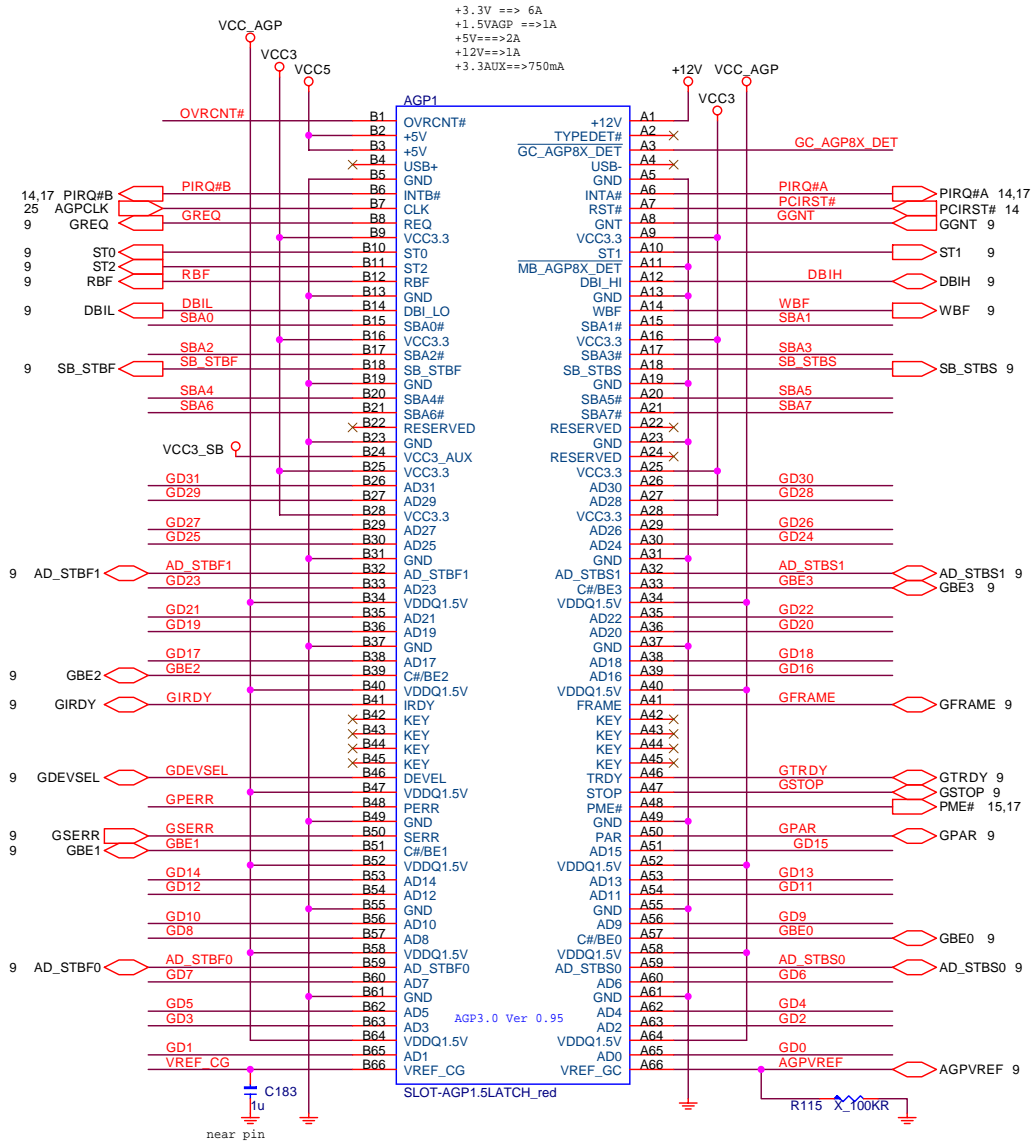






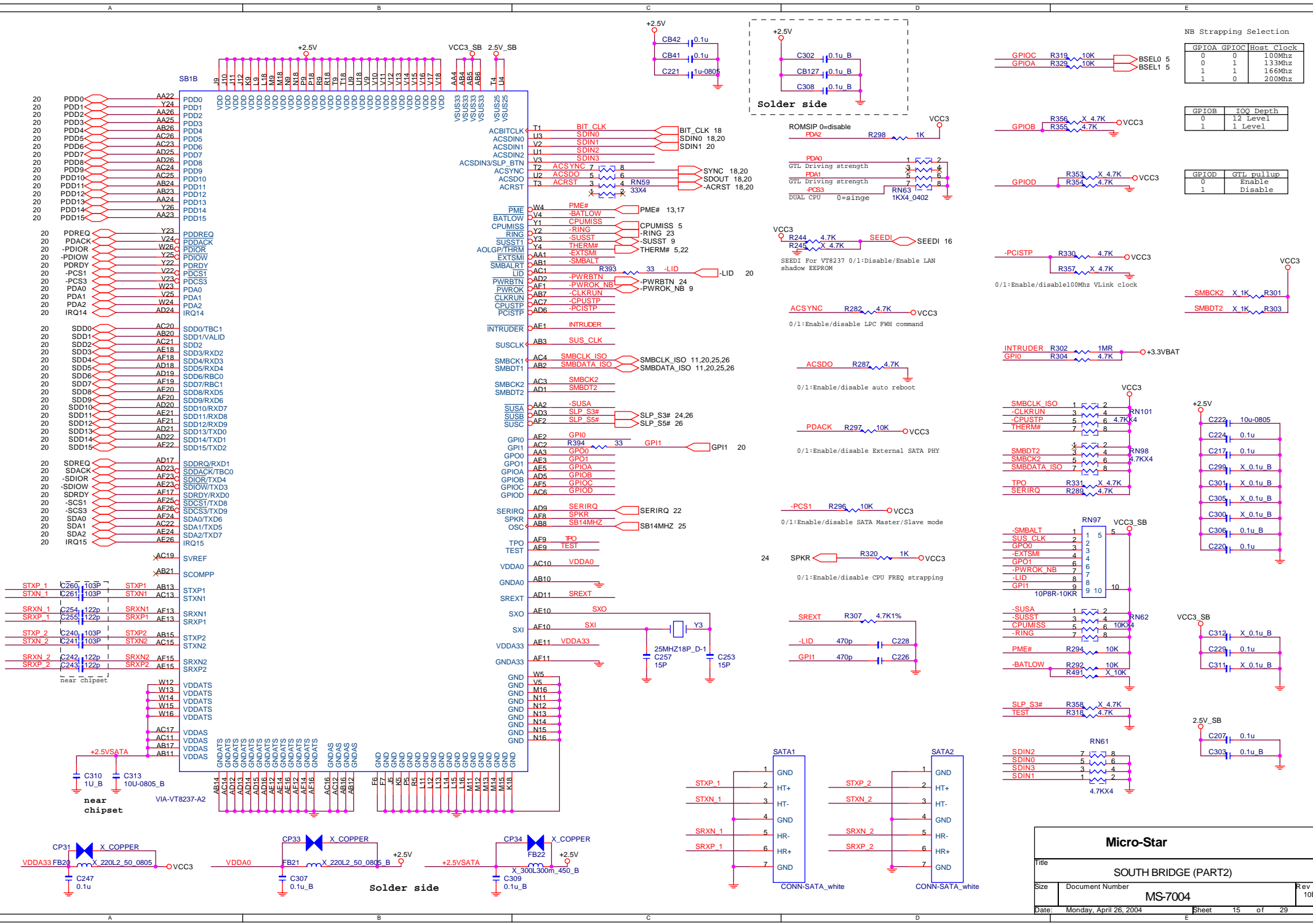


9 SBA[0:7] SBA[0:7]
9 GD[0:31] GD[0:31]



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AGPSLOT			
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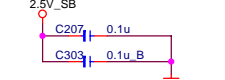
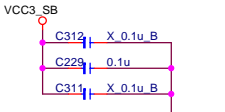
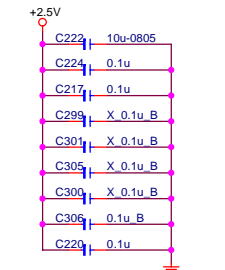
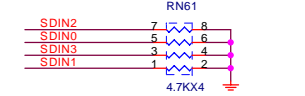
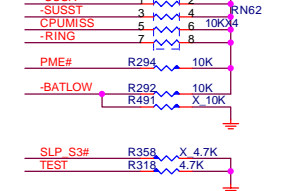
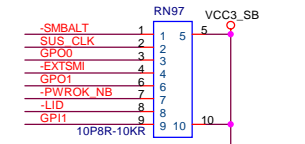
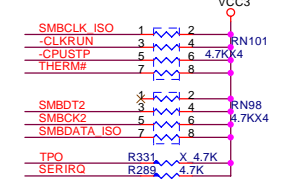
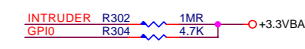
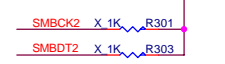
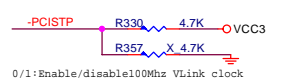
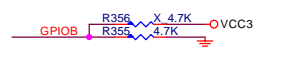


NB Strapping Selection

GPIOA	GPIOC	Host Clock
0	0	100Mhz
0	1	133Mhz
1	1	166Mhz
1	0	200Mhz

GPIOB	IOQ Depth
1	1 Level

GPIOD	GTL pullup
0	Enable
1	Disable

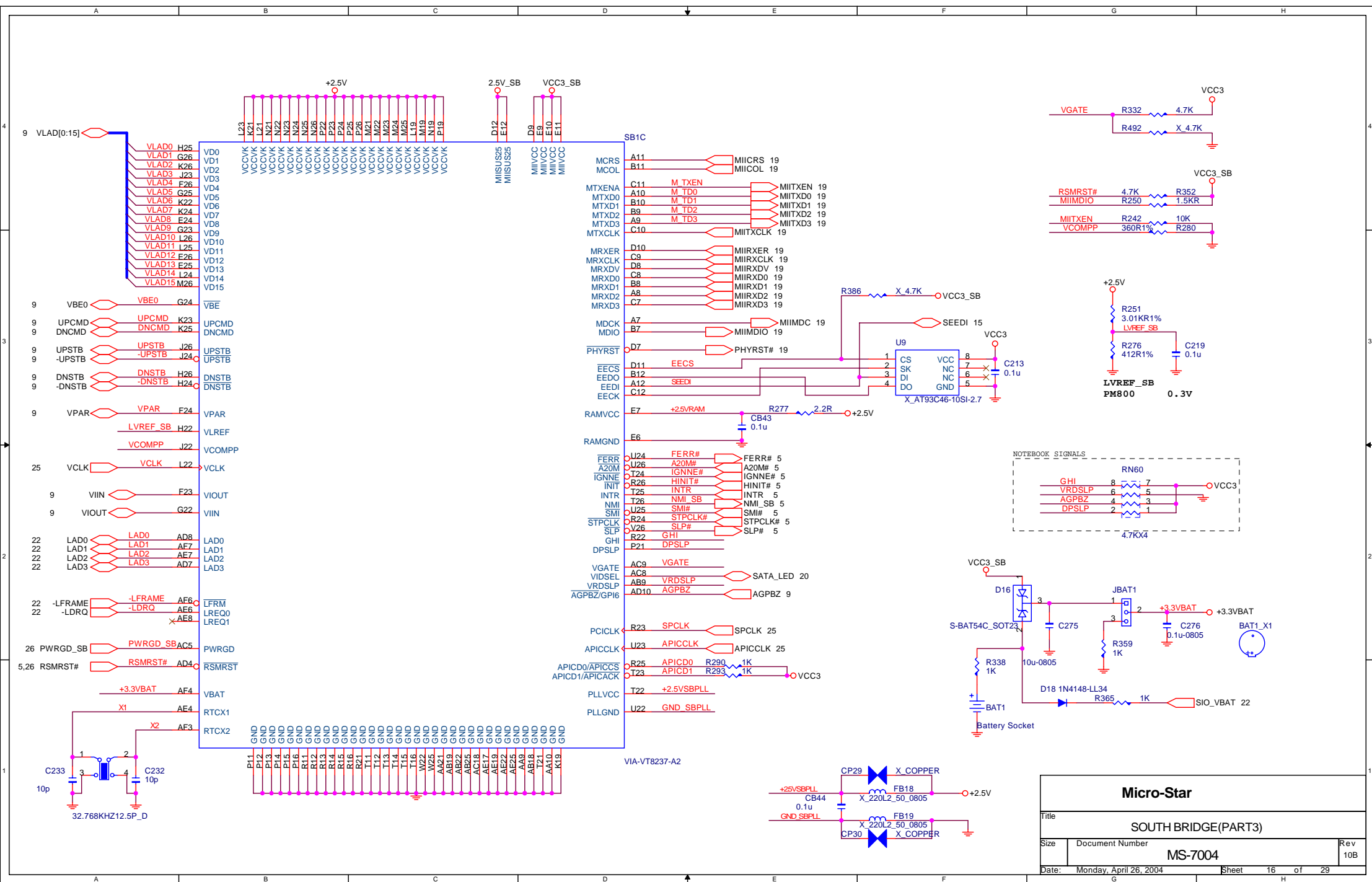


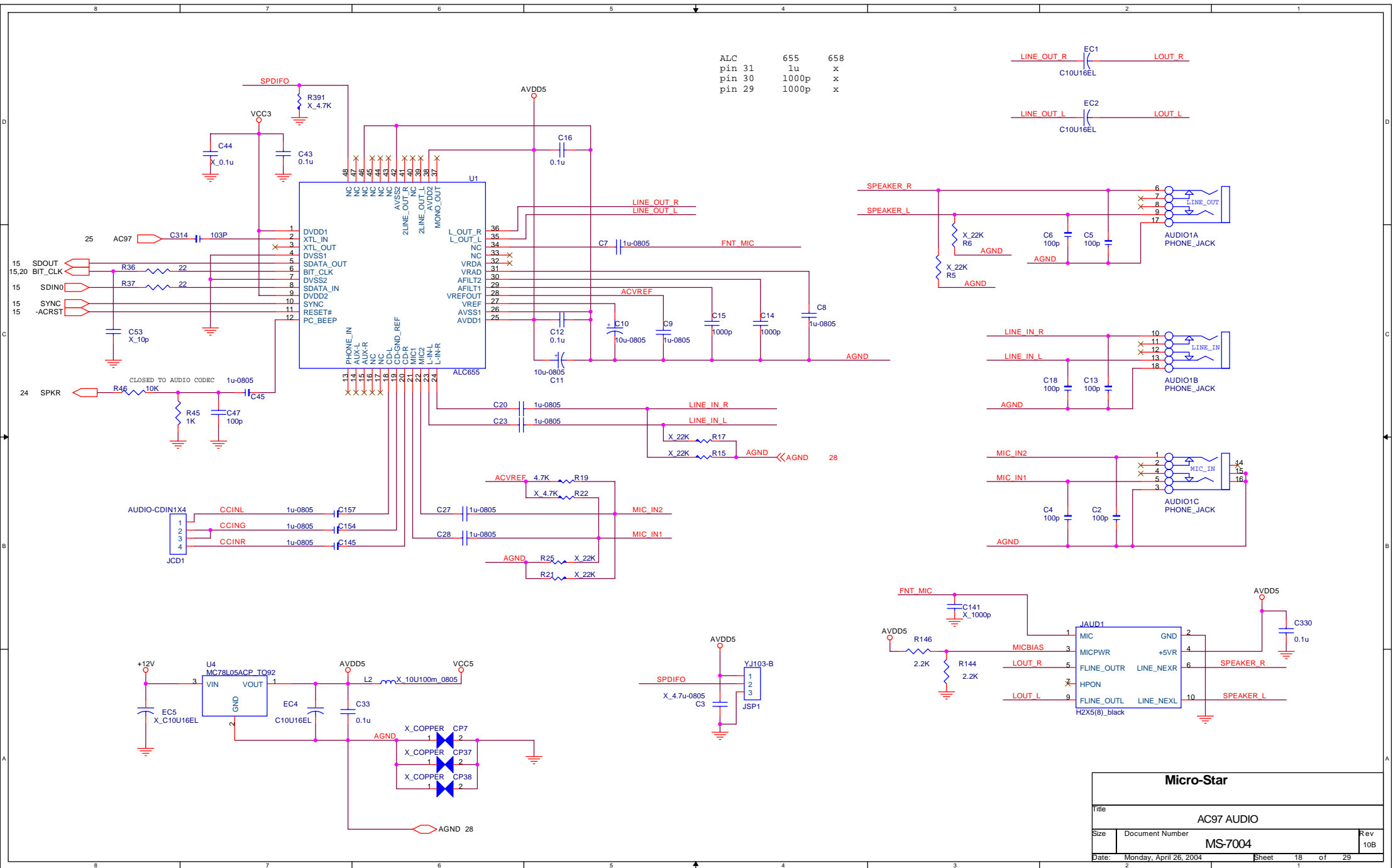
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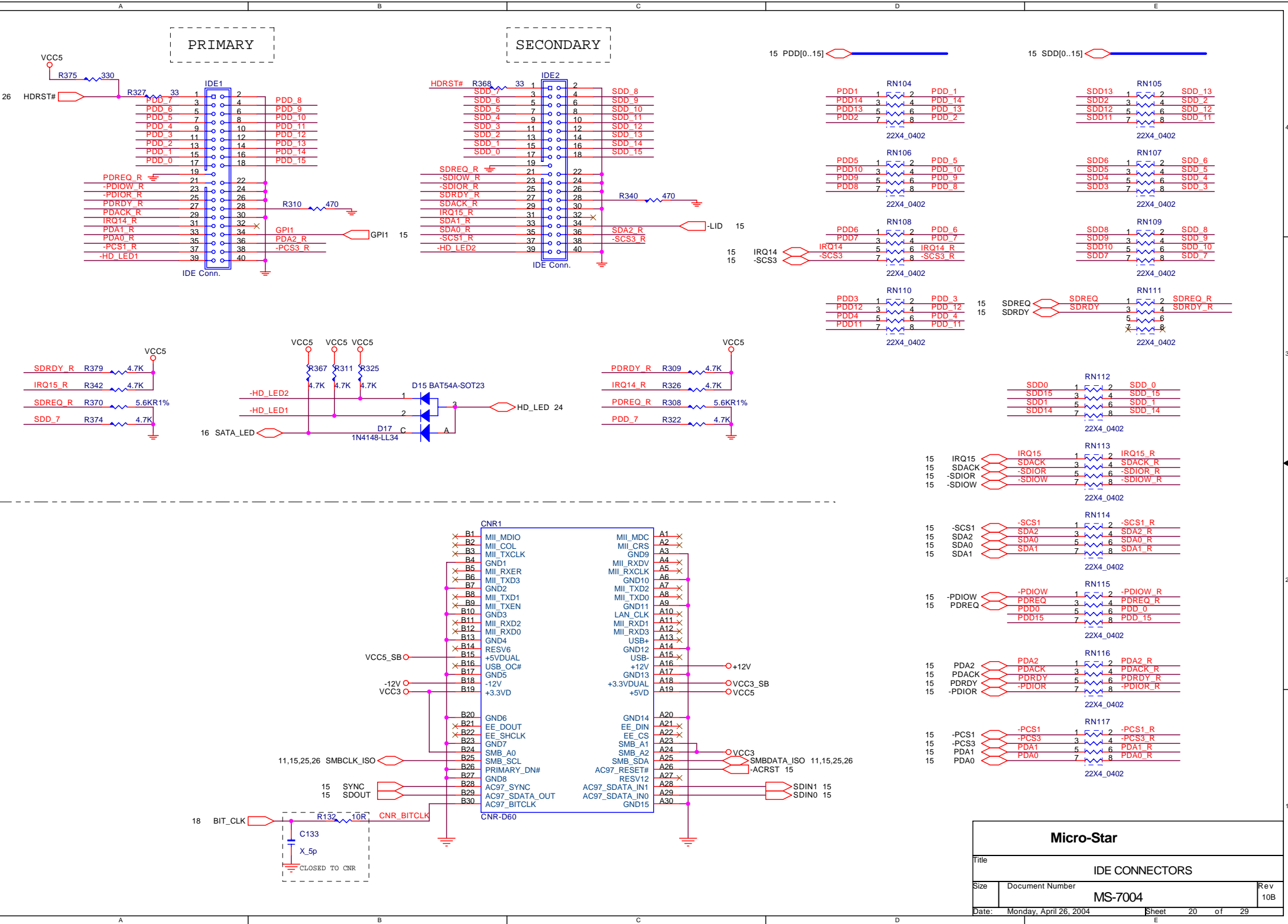
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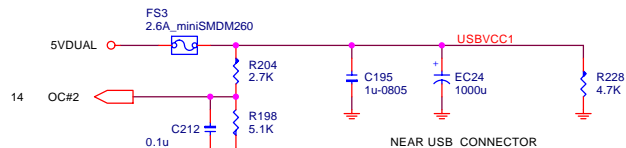
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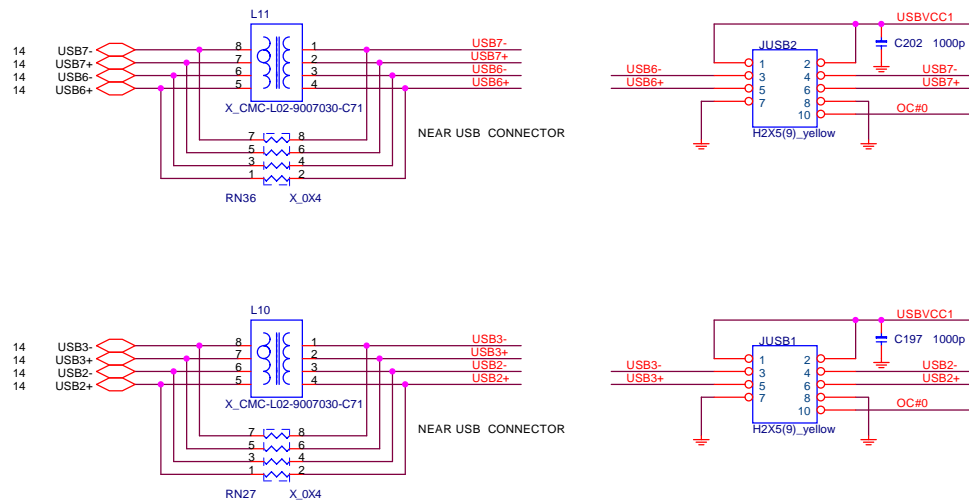




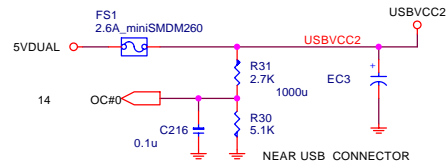
POWER CIRCUIT FOR USB PORT 4,5,6,7



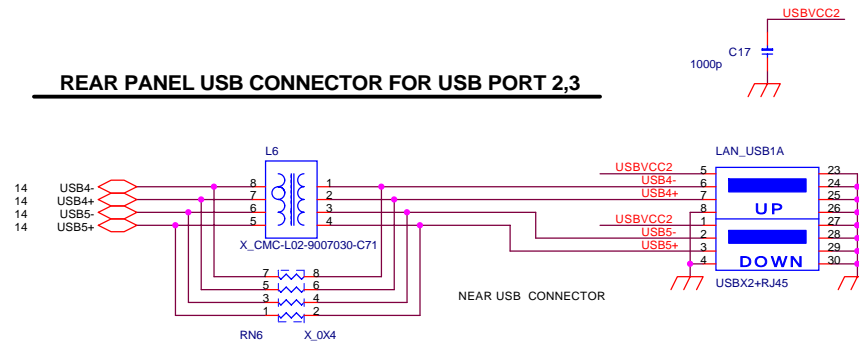
REAR PANEL USB CONNECTOR FOR USB PORT 4,5,6,7



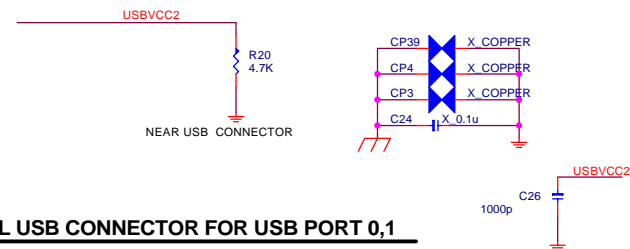
POWER CIRCUIT FOR USB PORT 2,3



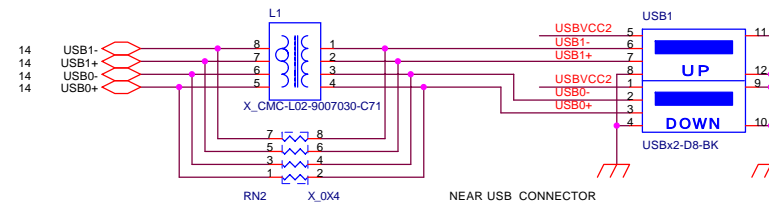
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



POWER CIRCUIT FOR USB PORT 0,1

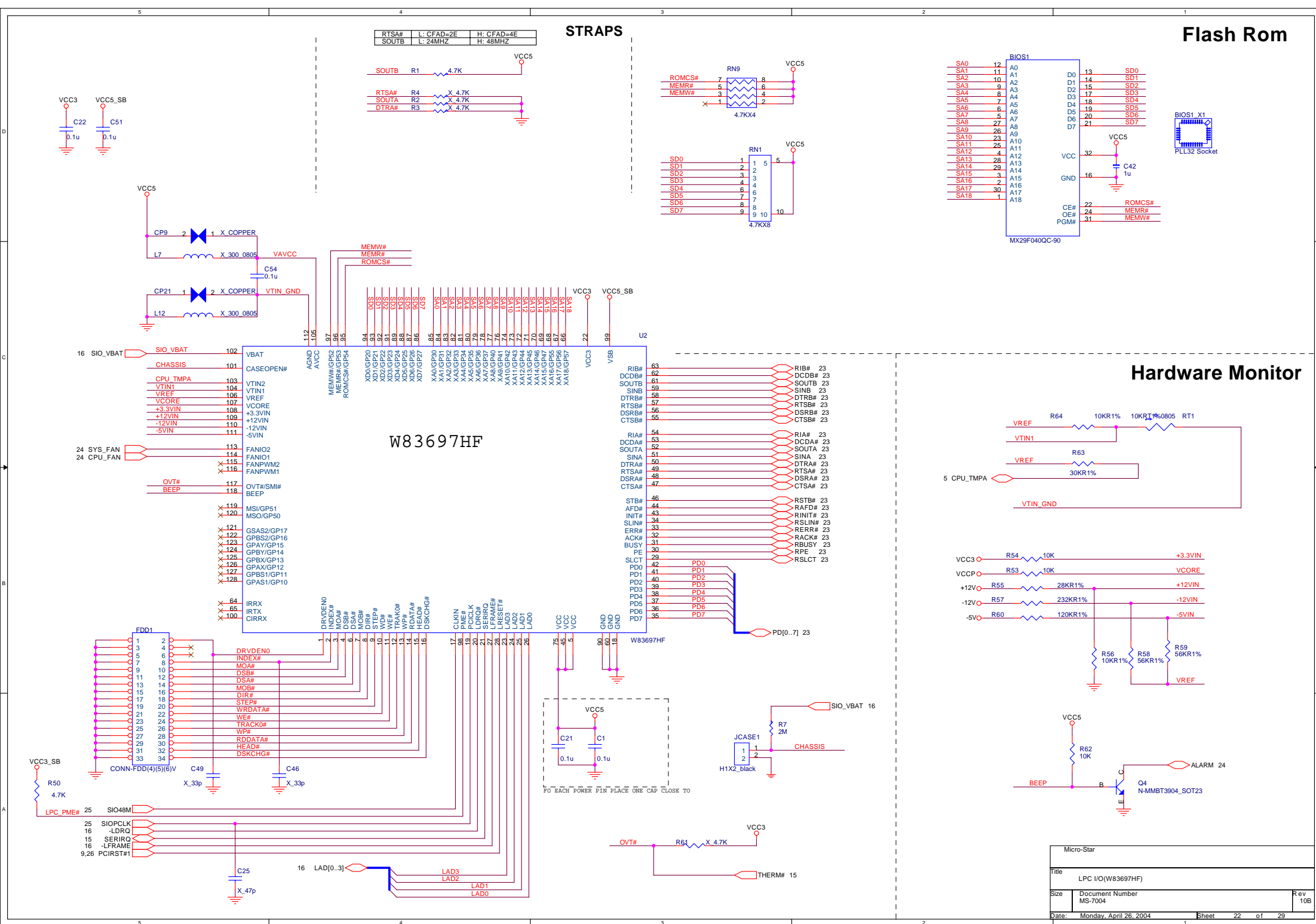


REAR PANEL USB CONNECTOR FOR USB PORT 0,1

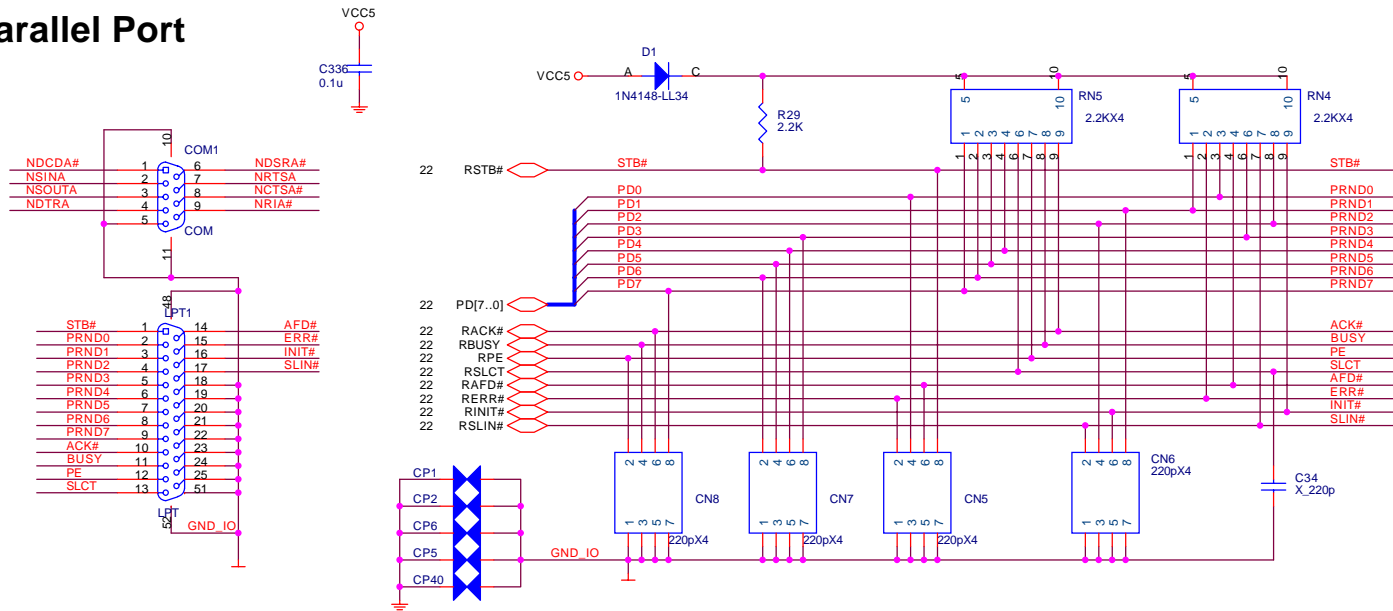


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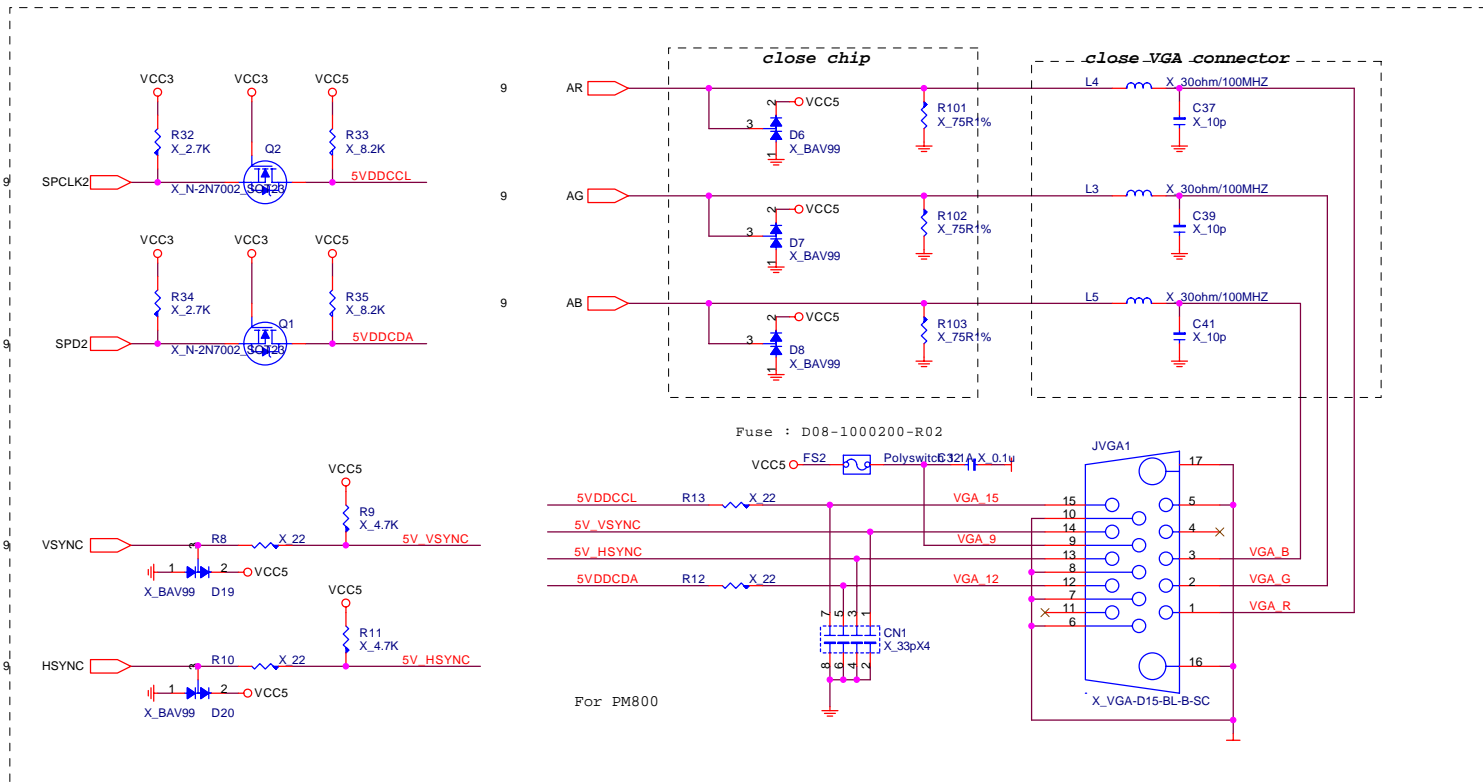
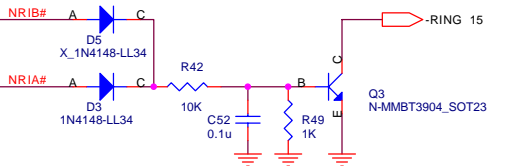
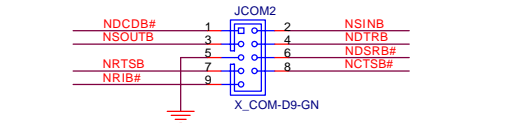
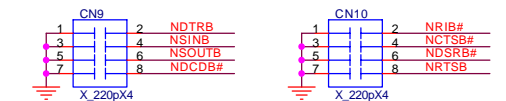
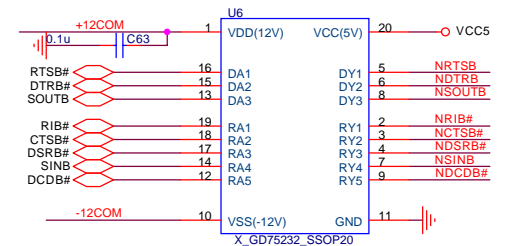
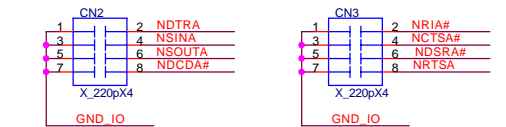
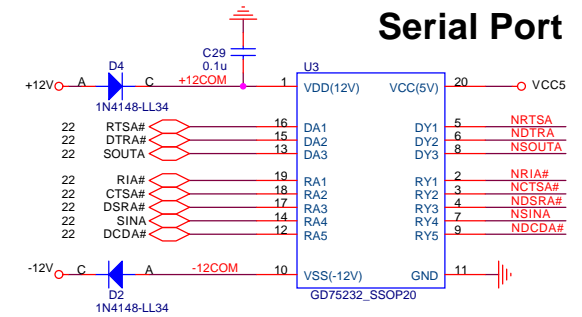
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USB Connectors		
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Parallel Port

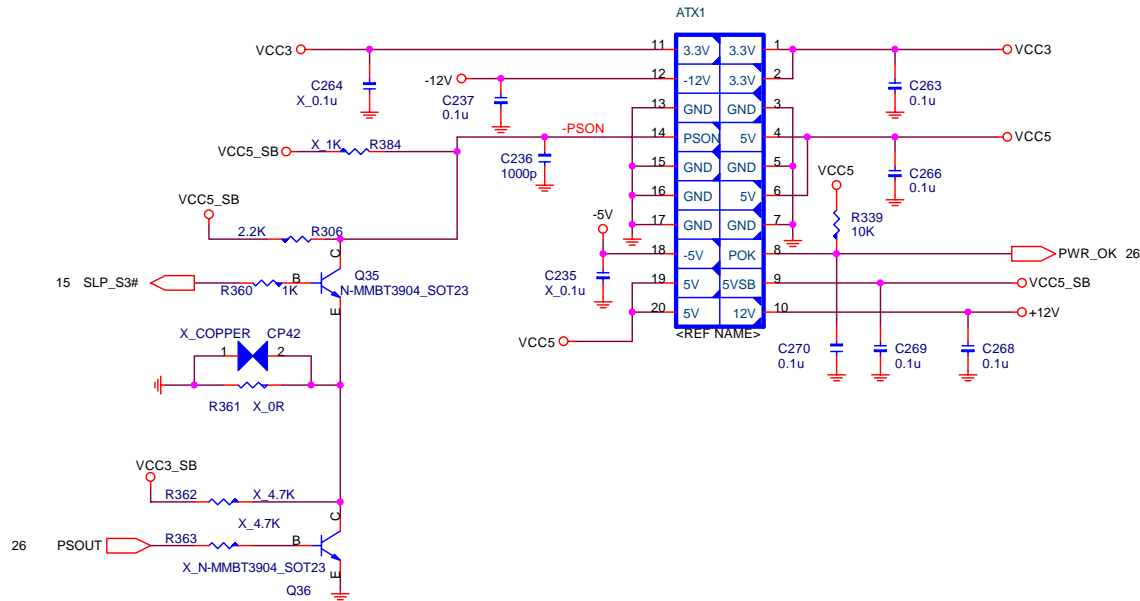


Serial Port

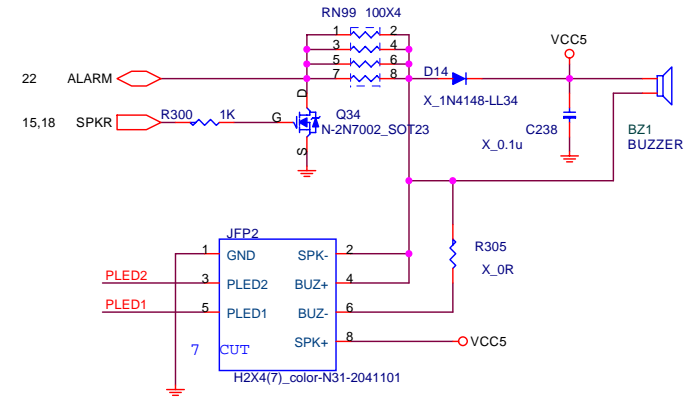


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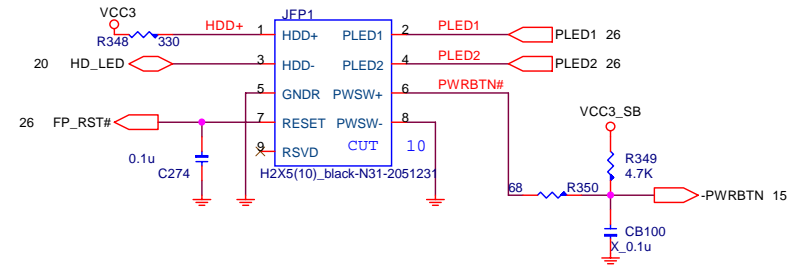
ATX Connector



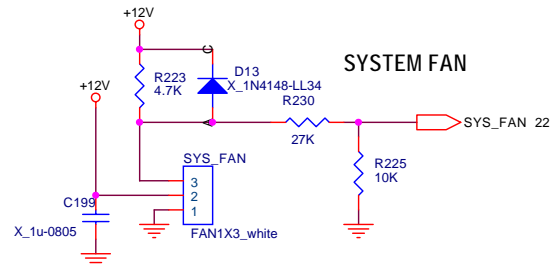
MSI Front Panel Connector



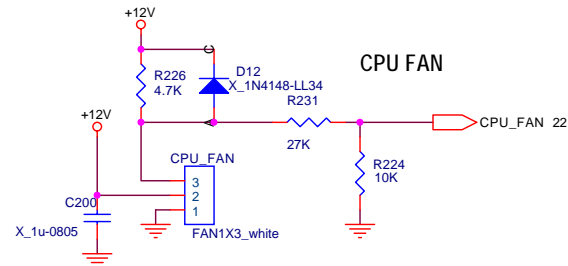
INTEL/PB Front Panel Connector



SYSTEM FAN

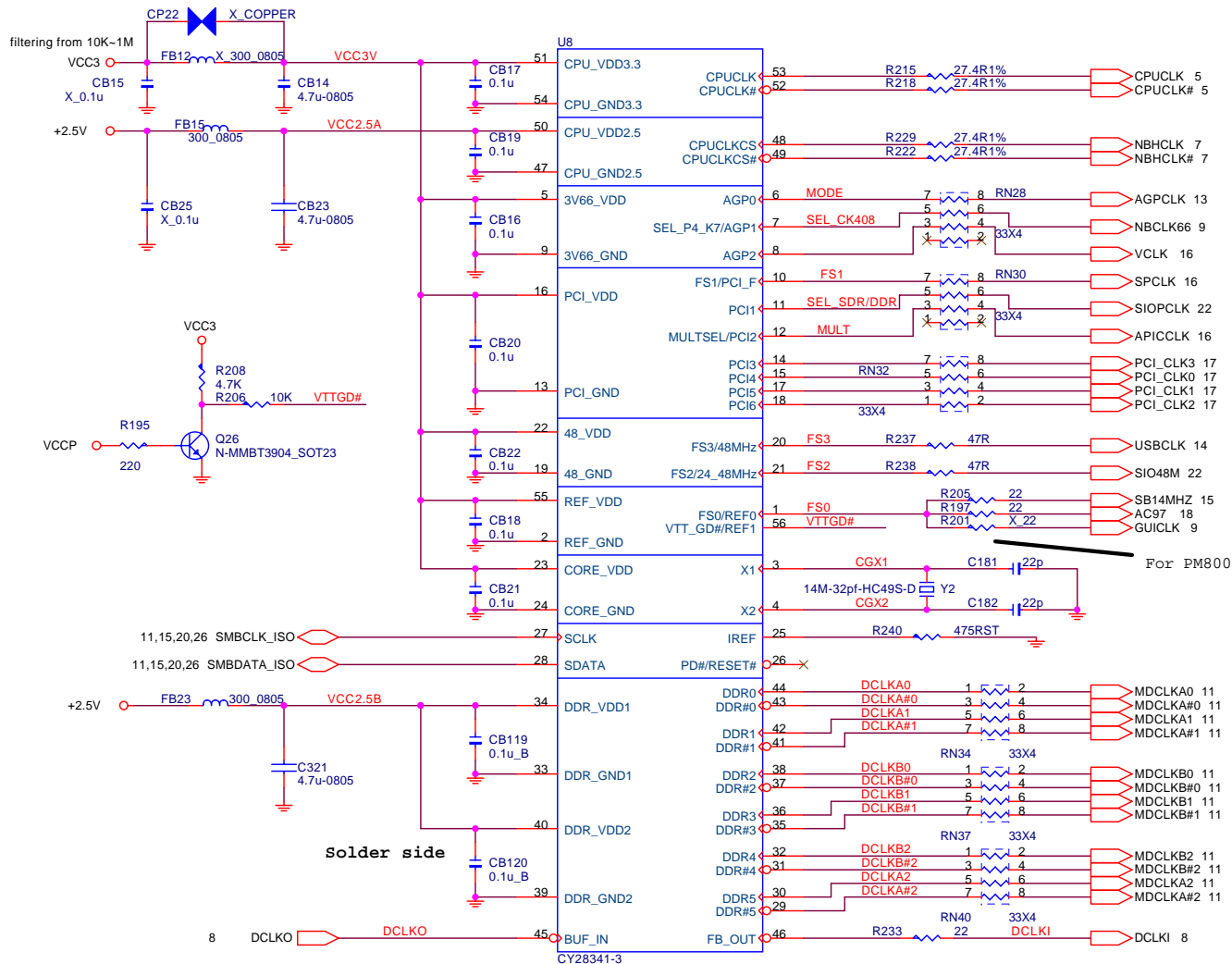


CPU FAN

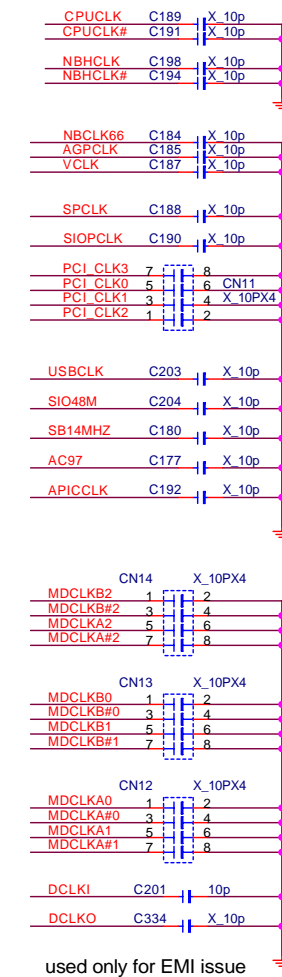


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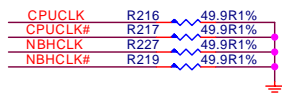
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ATX Connector & Front Panel			
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Pull-Down Capacitors

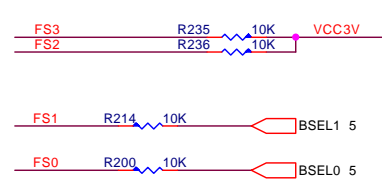


Shut Source Termination Resistors

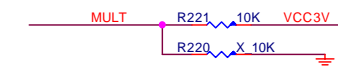
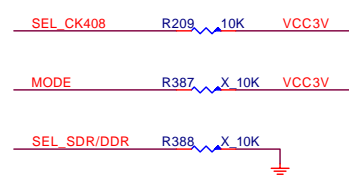


Trace less 0.2" 49.9ohm for 50ohm M/B impedance

CLOCK STRAPPING RESISTORS



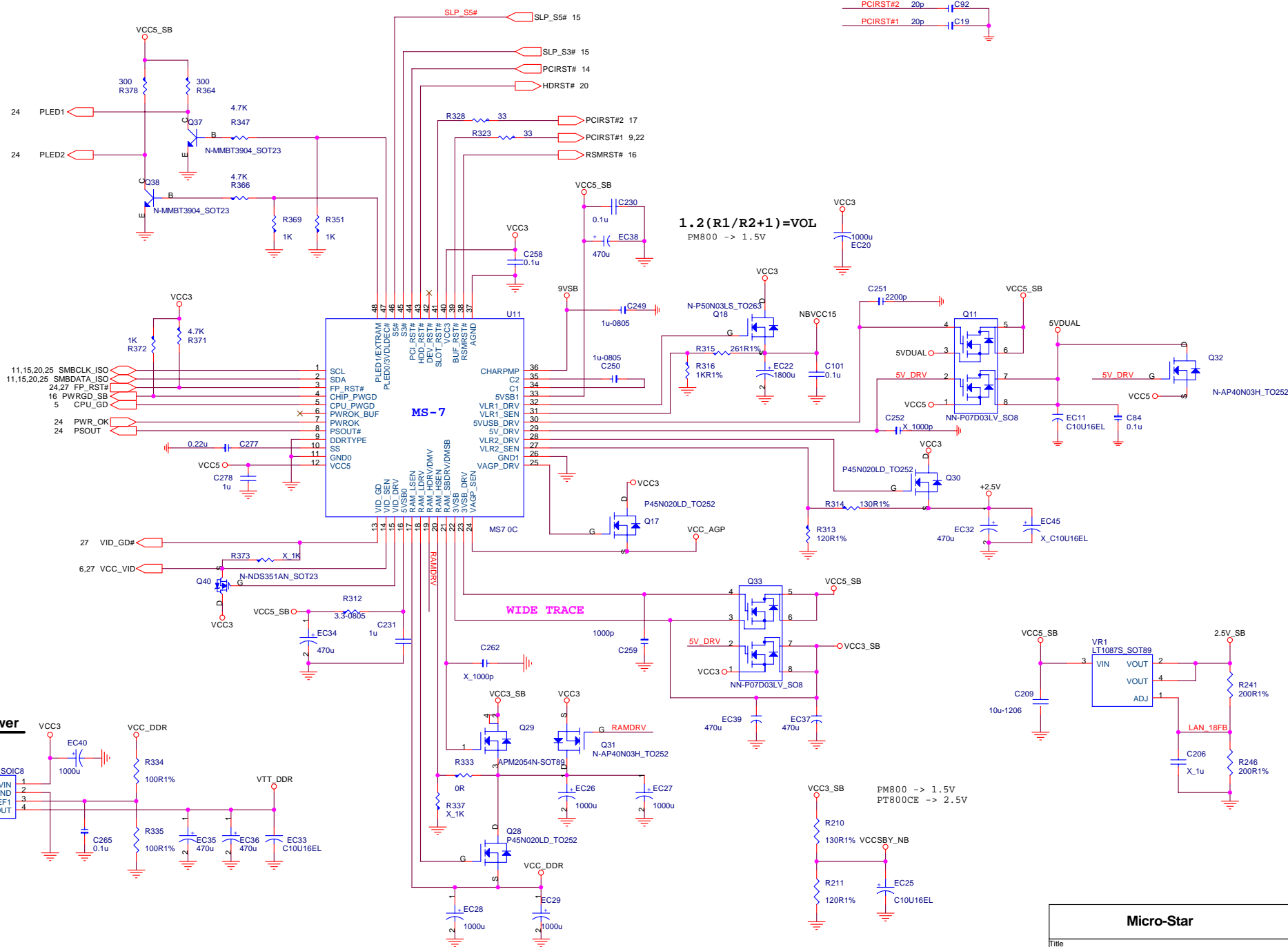
FS3	FS2	FS1	FS0	FSB (MHz)
1	1	0	0	100 MHz
1	1	0	1	133 MHz
1	1	1	0	200 MHz
1	1	1	1	166 MHz

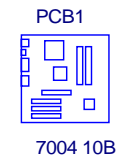
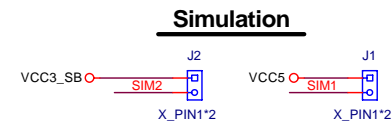
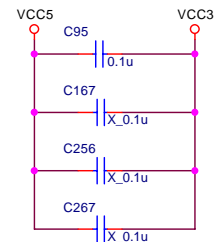
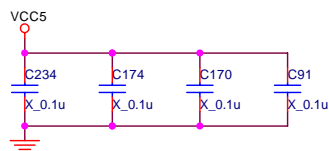
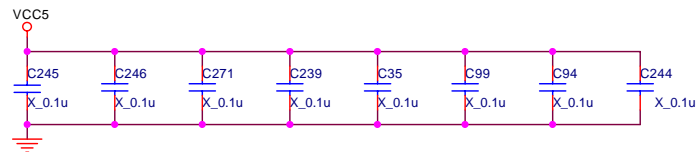
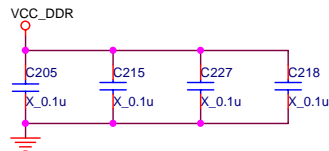
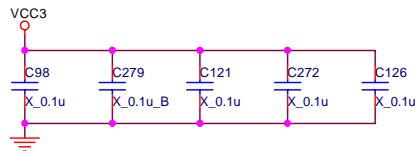


MULT	Rr	Iref	Ioh	Voh
0	221	5.00mA	4*Iref	1.0V
1	475	2.32mA	6*Iref	0.7V

Micro-Star

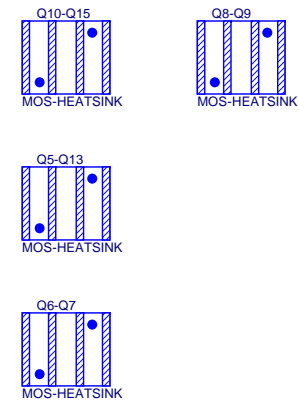
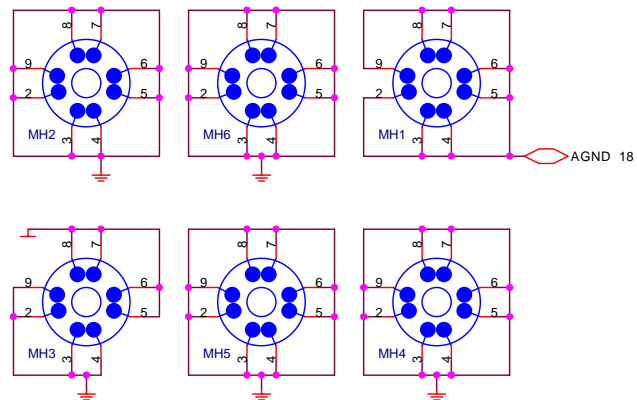
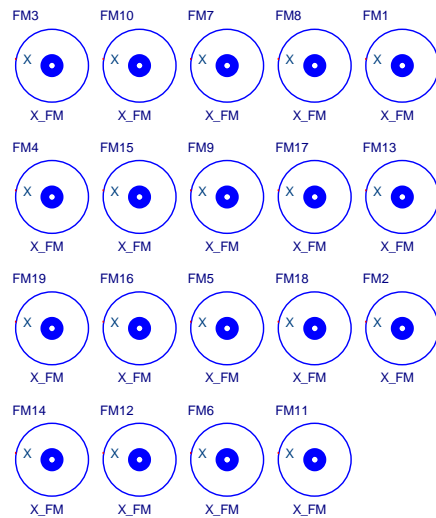
Clock Generator





Mounting Holes

Optics Orientation Holes



Micro-Star			
Title			
EMI PART			
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		1	Rev 10B

MS-7004 VOC

- 1.北橋ballout change to PM800/PT800 VER:B , Add 電源Pin .
- 2.Modify PWM layout & placemant .
- 3.Modify CPU & CHIPS 電源VCCP.NBVCC15內層切割.
- 4.Delete 預留VT8235CE的電阻.
- 5.Delete U5(Transform),改用有包進去的Lan connector .
- 6.BIOS ROM 與 FANCPU1 卡機構問題 & CPUFAN 與 SYSFAN 互換
- 7.Modify NB VCCDAC & VCCPLL u路.
- 8.NB 電源背焊電容改成10u/0805.
- 9.Modify U8(Clock Generator)電源線路,Add ICS strapping resistors.
- 10.加粗VCC5_SB & VCC3_SB切內層

MS-7004 v100

- | |
|------------------------------------------------------------|
| 1.Modify net VID_GD# circuit |
| 2.Change some resistors & cap for VRM transient. |
| 3.加寬 net CPU_TMPA(CPU to I/O) & VCCP_IN(JPW1 to PU1) |
| 4.Modify VRM layout |
| 5.ADD NB pin Y6,AB5,AB6 pull down resistors & pin N3接地 |
| 6.DDR BUS 0 ohm 直接短路 |
| 7.C92,C19移至U11端,ADD C334 for net DCLKO |
| 8.Bios Rom VCC5 trace 拉至C42 |
| 9.R389,R390,R249,R361 直接短路,cost down 0 ohm |
| 10.USB 0 ohm 排阻直接短路 |
| 11.Modify VCC5 Plane for IDE BUS 跨切割 |
| 12.VCC5 trace 拉粗至12~25 mils |
| 13.Modify net CPU_GD & VCC_VID & VCC_AGP_SEN & VTIN_GND 走線 |

MS-7004 V10A

- 1.ADD IDE 排阻
- 2.Modify LAN 10/100 燈號線路
- 3.Modify VRM 切割
- 4.Delete JSLP1
- 5.Modify +2.5V 切割區 & USB 5VDAUL 切割區
- 6.change USB Rset >>> 5.9K & VGA Rset >>> 82 ohm
- 7.ADD C335 20P for 北橋 PCIRST#1
- 8.LVREF_SB >>> 0.3V (R276 >>> 412ohm)

10B

Apr. 12

1. Page 15 : change R307 to 4.7K 1%.
2. Page 10 : change CB107, CB117, CB115, CB104, CB105, C290, C291, C292 to 22u 0805; add CB129, CB130.
3. Page 14 : add R490.
4. Page 15 : add R491.
5. Page 16 : add R492.

Apr. 15

1. Page 25 : change R233 to 22, C201 to 10p.
2. Page 12 : delete MD, DQS, DQM damping R.

Apr. 15

1. Page 12 : rearrange resistors, R-packs.